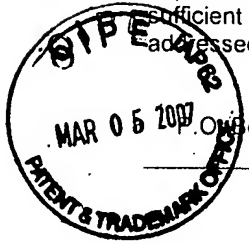


HW

I hereby certify that this correspondence is being deposited with the United States Postal Service, with sufficient postage, as first class mail in an envelope addressed to:



Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450, Alexandria, Virginia 22313-1450
on February 28, 2007
Date of Deposit

Jason M. Wejnert, Reg. No. 55,722

Name of applicant, assignee or
Registered Representative

Jason M. Wejnert

Signature
February 28, 2007
Date of Signature

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Appln. of: KOEDER et al.

Appln. No.: 10/518,291

Filed: December 16, 2004

For: METHOD FOR ALTERING
DESIGN DATA FOR
PRODUCING A COMPONENT,
AND ASSOCIATED UNITS

Attorney Docket No: 10808/195 (In1242WOUS)

Examiner: Not yet assigned

Group Art Unit: 2825

SECOND SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

In accordance with the duty of disclosure under 37 C.F.R. §1.56 and §§1.97-1.98, and more particularly in accordance with 37 C.F.R. §1.97(b), Applicants hereby cite the following references:

OTHER ART

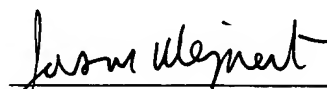
German Office Action dated October 24, 2006 [cited in claimed corresponding German Application No. DE 102 26 915.7].
Non-certified English translation of the German Office Action dated October 24, 2006.
Brück, Rainer, "Entwurfswerkzeuge für VLSI-Layout," "Methoden und Algorithmen für den rechnergestützten Entwurf von VLSI-Layout," pp. 140-143.
Non-certified English translation of the article by Brück, Rainer, "Entwurfswerkzeuge für VLSI-Layout," "Methoden und Algorithmen für den rechnergestützten Entwurf von VLSI-Layout," pp. 140-143.
Bourai et al., "Layout Compaction for Yield Optimization via Critical Area Minimization," Electrical Engineering Department, University of Washington, ACM, 2000, pp. 122-125.

Applicants are enclosing Form PTO-1449 (one sheet), along with copies of cited references C1-C5. Applicants respectfully request the Examiner's consideration of the above references and entry thereof into the record of this application.

By submitting this Statement, Applicants are attempting to fully comply with the duty of candor and good faith mandated by 37 C.F.R. §1.56. As such, this Statement is not intended to constitute an admission that any of the enclosed references, or other information referred to therein, constitutes "prior art" or is otherwise "material to patentability," as that phrase is defined in 37 C.F.R. §1.56(a).

Applicants have calculated no fee to be due in connection with the filing of this Statement. However, the Director is authorized to charge any fee deficiency associated with the filing of this Statement to a deposit account, as authorized in the Transmittal accompanying this Statement.

Respectfully submitted,



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